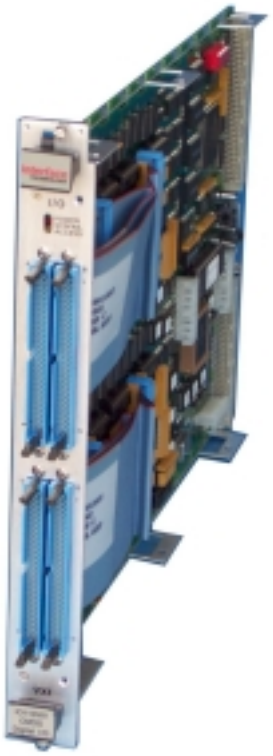
SR5020

TTL I/O Module For SR5000 Digital Test Subsystem



- 32 Input and 32 Output Pins per Module
- 64K Vectors per Channel
- RAM-Backed and Algorithmic Pattern Generation
- NRZ, RZ, RONE, RTC, and RI Output Data Formats Supported
- 16 Stimulus Timing Generators per Module
- Two Response Timing Generators per Module
- 100 ps Edge Placement Resolution

High Channel Density

The SR5020 TTL I/O Module provides 32 stimulus pins and 32 response pins in a single C-size slot. Up to 20 SR5020 I/O modules may be controlled by the SR5010 Timing/Control Module for a total of 640 I/O pins. Input and output pins are grouped on separate connectors, providing the most efficient method of interfacing to the UUT. Bidirectional capability is accomplished by simply externally connecting the input pins to the output pins.

The SR5020 I/O Module contains seven separate memory banks, each 64K vectors in depth, for generating stimulus patterns, expected response patterns, and recording UUT response data.

The Stimulus Memories consist of the Output, Tristate and Algorithmic Output memories. The Output Memory contains the actual data patterns to be generated to the UUT. Tristate Memory provides tristate control which supports bidirectional I/O. The Algorithmic Output Memory determines which algorithmic pattern will be output.

The Response Memories consist of the Expect, Mask, and Algorithmic Expect memories. The Expect Memory contains the expected response data for the UUT and is the basis for input compare operations. The Mask Memory determines which patterns are to be ignored for input response comparison. Algorithmic Expect Memory determines which algorithmic expect pattern will be compared against the UUT input response.

Record Memory is used to store either the UUT response data or the result of the comparison between the UUT response data and the expected response pattern.

Data Formatting with Precise Edge Placement

Stimulus pins may be independently programmed for any of the following data formats: Non-Return to Zero (NRZ), Return to Zero (RZ), Return to One (R1), Return to Complement (RC), and Return to Inhibit/Tristate (RI).

Each SR5020 TTL I/O Module contains 16 timing generators for stimulus edge placement and pulse width timing. Output pins can select from 2 pairs of timing generators to define the leading and trailing edges of each signal pin. Groups of eight output pins share an independent set of 2 timing generator pairs for a total of 8 stimulus timing generator sets per card. 100 ps edge placement resolution provides precise UUT timing for bus emulation testing, memory testing, and functional testing.

Response pins can select from 2 response timing generators to define the sample and compare edges, or the 2 response timing generators can be combined together for window compare with glitch detection.

*SR5020 SPECIFICATIONS**

Channels per Module:

Inputs	32
Outputs	32

Memory Types:

Stimulus	Output, Tristate, Algorithmic
Response	Expect, Mask, Algorithmic
Record	

Memory Depth:

65,500 vectors

Output Timing:

Clock Pairs (assert/deny)	8 total per card; 2 per 8 channels
Delay Range	one clock period
Resolution	100 ps, nonmonotonic 2 ns, monotonic
Delay Accuracy	±1 ns typ., ±2 ns max.
Output Pulse Width	Min: 10 ns Max: period clock - 10 ns
Pulse Width Accuracy	3.0 ns typ., 5.0 ns maximum

Skew:

Same Module	±1 ns typical, ±3 ns maximum
SR5020-SR5020	±2 ns typical, ±3 ns maximum

Data Formats:

RZ	Return to Zero
NRZ	Non-Return to Zero
RONE	Return to One
RC	Return to Complement
RI	Return to Inhibit/Tristate

Output Drivers:

Type	74F125
Voh	3.40 V, typical
Vol	0.55 V, typical
Sink Current	65 mA
Source Current	15 mA
Output Termination	100 ohms, series

Input Receivers:

Type	74ACT244
Vih	2.0 V, minimum
Vil	0.8 V, maximum
Input Impedance	10k ohms

Input Sample / Compare Modes:

Formats	Edge / window
Range	One period clock cycle
Resolution	100 psec
Accuracy	±1 ns typical; ±2 ns maximum

Input Timing:

Sample/Compare Clocks	2 per card (edge mode) 1 per card (window mode)
Input Delay Range	One clock period
Clock Separation	10 ns, min.
Resolution	100 ps, nonmonotonic 2 ns, monotonic

External Tristate Input:

Number	Four per module; byte control
Active Level	Low
Input Voltage	TTL
Enable time	125 ns
Disable time	150 ns
Input Impedance	1K ohms

VXI Specifications

Interface Compatibility:

Type	Register-based, servant only (controlled by SR5010)
Revision	1.3 and 1.4
Size	C-size, single slot
Configuration	Static
Memory	2 MB VME A32/D32

Power Requirements:

+5.0 volts	10.0 A (7.5 A	50 W at 50 MHz 37.5 W at 40 MHz)
-5.2 volts	4.0 A	20.8 W
+12.0 volts	0.1 A	1.2 W
-12.0 volts	0.1 A	1.2 W
-2.0 volts	2.0 A	4.0 W

Total Power		77.2 W at 50 MHz

Cooling Requirements:

Per-slot Average	65 W typical, 77 W maximum
Airflow	6 L/sec @ 0.38 mm water pressure for 10°C temperature rise

Environmental Specifications:

Temperature	Storage = -40°C to +75°C Operating = 0°C to +45°C
Humidity	5% to 95% relative, noncondensing

Software Drivers:

National Instruments	LabView
National Instruments	LabWindows/CVI

* Specifications subject to change without notice.

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